diffusion regions and a first control gate over said first floating gate, said second and third diffusion regions constituting a second memory cell having a second floating gate over a second channel region sandwiched between said second and third diffusion regions and a second control gate over said second floating gate;

forming a mask layer to cover a surface of said second diffusion region with leaving top surfaces of said first and second control gates and surfaces of said first and third diffusion regions uncovered;

forming a silicide layer on said top surface of said first and second control gates and said surfaces of said first and third diffusion regions, said surface of said second diffusion region being free from formation of said silicide layer by existence of said mask layer.

32. A method of manufacturing a semiconductor device, comprising:

selectively forming in a semiconductor substrate first, second, third, fourth, fifth and sixth diffusion regions apart from one another, said first and second diffusion regions constituting a first memory cell having a first floating gate over a first channel region sandwiched between said first and second diffusion regions and a first control gate over said first floating gate, said second and third diffusion regions constituting a second memory cell having a second floating gate over a second channel region sandwiched between said second and third diffusion regions and a second control gate over said second floating gate, said fourth and fifth diffusion regions constituting a third memory cell having a third floating gate over a third channel region sandwiched between said fourth and fifth diffusion regions and a third control gate over said

third floating gate, said fifth and sixth diffusion regions constituting a fourth memory cell having a fourth floating gate over a fourth channel region sandwiched between said fifth and sixth diffusion regions and a fourth control gate over said fourth floating gate;

forming a mask layer to cover a surface of said second and fifth diffusion regions with leaving top surfaces of said first, second, third and fourth control gates and surfaces of said first, third, fourth and sixth diffusion regions uncovered;

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forming a silicide layer on said top surface of said first, second, third and fourth control gates and said surfaces of said first, third, fourth and sixth diffusion regions, said surfaces of said second and fifth diffusion regions being free from formation of said silicide region by existence of said mask layer.

33. The method as claimed in claim 31, wherein said forming said mask layer comprises forming an insulating film on said semiconductor substrate and etching back said insulating film to expose said top surfaces of said first and second control gates and said surfaces of said first and third diffusion regions.

34. The method as claimed in claim 33, further comprising forming side wails on side surfaces of said first control gate and said first floating gate of said first memory cell and side surfaces of said second control gate and said second floating gate of said second memory cell, said side wails facing each other over said second diffusion region, wherein a space on said second diffusion region sandwiched said side wails is filled with said mask layer.

35. The method as claimed in claim 32, wherein said forming said mask layer comprises forming an insulating film on said semiconductor substrate and etching back said insulating film to expose said top surfaces of said first, second, third and fourth control gates and said surfaces of said first, third, fourth and sixth diffusion regions.

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36. The method as claimed in claim 35, further comprising forming side walls on side surfaces of said first control gate and said first floating gate of said first memory cell, side surfaces of said second control gate and said second floating gate of said second memory cell, side surfaces of said third control gate and said third floating gate of said third memory cell and side surfaces of said fourth control gate and said fourth floating gate of said fourth memory cell, said side walls of said first and second memory cells facing each other over said second diffusion region, said side walls of said third and fourth memory cells facing each other over said fifth diffusion region, wherein a space on said second diffusion region sandwiched said side walls of said first and second memory cells is filled with said mask layer.

37. The method as claimed in claim 36, wherein a distance between said side surfaces of said first and second memory cells facing each other over said second diffusion region is smaller than a distance between said side surfaces of said third and fourth memory cells facing each other over said fifth diffusion region.

38. The method as claimed in claim 32, further comprising:

forming an interlayer film over said semiconductor substrate after forming said silicide layer;

forming a source line wiring on said interlayer film and a source contact connecting said source line wiring with said silicide layer on said fifth diffusion region.